**University of Texas at San Antonio**
**Department of Electrical and Computer Engineering**
**EE 4243 – Computer Organization and Architecture**

**Fall 2018 Syllabus**

**Part A – Course Outline**

**Required Course in Computer Engineering**

**Catalog description:**
Computer Organization and Architecture (2-3) 3 hours credit. Prerequisites EE3463 and EE3563. Design of advanced state machines and computer systems, and processor design using computer- assisted design and analysis tools.

**Prerequisites:**
- EE3463 Digital System Design and
- EE3563 Microcomputer Systems I

**Textbook:**
- Computer Organization and Design: The Hardware/Software Interface (RISC-V Edition), David Patterson and John Hennessy, Morgan Kaufmann, 2017.

**Optional Materials:**
- Digital Design and Computer Architecture, David Money Harris and Sarah L. Harris, 2nd Edition, Morgan Kaufmann.
- Computer Architecture: A Quantitative Approach, John Hennessy and David Patterson, 5th Edition, Morgan Kaufmann.
- There are two additional books that students may find useful for the lab assignments: one provides background on Verilog while the other provides background on the MIPS architecture.
    - Verilog Book – *"Verilog HDL: A Guide to Digital Design and Synthesis, 2nd ed.,"* by S. Palnitkar (Prentice Hall, 2003) provides a good introduction to Verilog-2001 well suited for the beginner.
    - MIPS Book – *"See MIPS Run Linux, 2nd edition,"* by D. Sweetman (Morgan Kaufmann, 2006) is a great book about the MIPS instruction set and the hardware/software interface specifically with respect to running the Linux operating system.

**Prerequisites by Topic:**
- Basic knowledge of combinational network design
- Basic knowledge of sequential network design
- Basic knowledge of microprocessors, machine languages, and computer Programming

**Course Objectives:**

- To develop an understanding of the architecture of computer systems. [b]
- To develop an understanding of ISAs (Instruction Set Architectures), microarchitecture to implement the ISA, datapath and pipelining. [b]
- To learn memory hierarchies, caches and virtual memory. [i]
- To use design tools in the designing of a processor. [j]

**Topics Covered:**

- Digital Building Blocks
- Computer Design Methodologies
- CPU and Instruction Set Design
- CPU Control Design
- Memory Organization
- Pipelining
- Superscalar Processors

**Class/Laboratory schedule:**

- Two 50-minute lecture sessions/week and one 2 hours and 45 minutes lab session/week

**Relationship to student outcomes:**

This course primarily contributes to the student outcomes:

(4) an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.

(6) an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.

(7) an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

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**Part B - General Course Information and Policies**

**Instructor:**
Lide Duan
Assistant Professor
Department of Electrical and Computer Engineering
University of Texas at San Antonio

**Office**: AET 2.376
**Phone**: 210-458-5208
**Email**: lide.duan@utsa.edu
**Webpage:** http://utsa-salsa.org

**Class Meeting Time**s: 5:30 to 6:20PM (Tuesdays and Thursdays)
**Lab Sessions**: 5 to 7:45PM (Wednesdays)
**Class/Lab Location**: EB 2.04.22
**Office Hours**: 3 to 5PM (Tuesdays and Thursdays) or by appointment.

**Website**:
All course materials will be handled electronically through the UTSA Blackboard Learn system. These include:

- Slides, HW, solutions, and other course materials distributed by the instructor.
- Notifications sent out by the instructor to all student emails.
- HW submissions by students.

**Textbook** (required):

- Computer Organization and Design: The Hardware/Software Interface (RISC-V Edition), David Patterson and John Hennessy, Morgan Kaufmann, 2017.

**Course Topics** (tentative):

- Fundamentals of computer architecture
- Architecture (instruction set architectures or ISA, RISC-V programming)
- Computer arithmetic
- Microarchitecture (single-cycle processor, multicycle processor, pipelined processor, branch prediction, superscalar, performance analysis, etc.)
- Memory systems (caches, main memory, virtual memory)

**Evaluation Method**:

- HW assignments: 30% (three assignments at 10% each)
- Exams: 35% (Exam 1 at 10%, Exam 2 at 10%, and the Final Exam at 15%)

- Quizzes: 5% (The instructor will randomly choose a few classes to have simple in-class quizzes. These are mainly for checking attendance. No make-up quizzes.)
- Lab: 30% (taught and graded by the TA).
- Total: 100%.
- After a grade (of a HW/exam/quiz) is posted, you will have up to a week to see me for any errors. After that, the grade is finalized.

**Grading Policy**:

- A student will get an A (including A+, A, and A-) if his/her final weighted total score is >= 90 **OR** he/she is ranked within the top 40% of all students.
- A student will get a B (including B+, B, and B-) if he/she cannot get an A but his/her final weighted total score is >= 80 **OR** he/she is ranked within the top 80% of all students.
- A student will get a C if he/she cannot get a higher letter grade but his/her final weighted total score is >= 70.
- A student will get a D if he/she cannot get a higher letter grade but his/her final weighted total score is >= 60.
- A student will get an F if his/her final weighted total score is below 60.

**About the HW Assignments**:

- There will be three HW assignments; each is assigned and due before an exam.
- HW questions are good examples of exam questions.
- All assignments must be submitted in pdf through Blackboard Learn before the specified deadlines. There will be no delay policy, and submissions missing the deadline will not be graded.
- No copying is allowed on any assignment. All parties involved (either copying or being copied) will lose all the points for the assignment.

**About the Exams**:

- Tentatively, Exam 1 will be on Thursday 9/20 (class time); Exam 2 will be on Thursday 10/25 (class time); and the Final Exam (comprehensive) will be scheduled later.
- All exams are close-book unless specified otherwise.
- No make-up exams (except for extremely special situations with legitimate proof and under discretion of the instructor).

## THE ROADRUNNER CREED

The University of Texas at San Antonio is a community of scholars, where integrity, excellence, inclusiveness, respect, collaboration, and innovation are fostered.

As a Roadrunner, I will:

- Uphold the highest standards of academic and personal integrity by practicing and expecting fair and ethical conduct;
- Respect and accept individual differences, recognizing the inherent dignity of each person;
- Contribute to campus life and the larger community through my active engagement; and
- Support the fearless exploration of dreams and ideas in the advancement of ingenuity, creativity, and discovery.
- Guided by these principles now and forever, I am a Roadrunner!

**The University of Texas at San Antonio Academic Honor Code**

**A. Preamble**

The University of Texas at San Antonio community of past, present and future students, faculty, staff, and administrators share a commitment to integrity and the ethical pursuit of knowledge. We honor the traditions of our university by conducting ourselves with a steadfast duty to honor, courage, and virtue in all matters both public and private. By choosing integrity and responsibility, we promote personal growth, success, and lifelong learning for the advancement of ourselves, our university, and our community.

**B. Honor Pledge**

In support of the ideals of integrity, the students of the University of Texas at San Antonio pledge:

"As a UTSA Roadrunner I live with honor and integrity."

**C. Shared responsibility**

The University of Texas at San Antonio community shares the responsibility and commitment to integrity and the ethical pursuit of knowledge and adheres to the UTSA Honor Code.